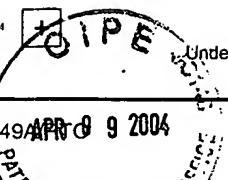


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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

				Application Number	10/061,459
				Filing Date	1/31/02
				First Named Inventor	Steven Teig, et al.
				Group Art Unit	2825
				Examiner Name	Thompson, Annette
Sheet	1	of	2	Attorney Docket Number	SPLX.P0091

U.S. PATENT DOCUMENTS

Examiner* Initials	Cite No. ¹	U.S. Patent Document Number	Kind Code ² (if known)	Date of Publication MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	1.	2002/0157 063	A1	10-24-2002	Besson	
	2.	2002/0178 432	A1	11-28-2002	Kim et al.	
	3.	2003/0145 288	A1	07-31-2003	Wang et al.	
	4.	4,703,435		10-27-1987	Darringer et al.	
	5.	5,003,487		03-26-1991	Drumm et al.	
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	14.	6,389,586	B1	05-14-2002	McElvain	
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	17.	6,446,240	B1	09-03-2002	Iyer et al.	
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	20.	6,470,486	B1	10-22-2002	Knapp	

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				Filing Date	1/31/02
				First Named Inventor	Steven Teig, et al.
				Group Art Unit	2825
				Examiner Name	Thompson, Annette
Sheet	2	of	2	Attorney Docket Number	SPLX.P0091

U.S. PATENT DOCUMENTS					
	21.	6,519,609	B1	02-11-2003	Touzet
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	23.	6,539,536	B1	03-25-2003	Singh et al.
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	25.	6,546,541	B1	04-08-2003	Petranovic et al.
	26.	6,618,835	B1	09-09-2003	Garlapati et al.

NON PATENT LITERATURE DOCUMENTS					
Examiner* Initials	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.			
	27.	NN78055443, "Automatic Remap", IBM Technical Disclosure Bulletin, Vol. 20, No. 12, May 1978, pp. 5443-5445 (5 pages).			
	28.	NN9411291, "Design of Portable Library using Parameterized Cells", IBM Technical Disclosure Bulletin, Vol. 37, No. 11, pp. 291-292 (4 pages).			
	29.	Markovic et al., "FPGA to ASIC Conversion Design Methodology with the Support for Fast Retargetting to Different CMOS Implementation Technologies", Proceedings of 2002 22 nd International Conference on Microelectronics", Vol. 2, 14 May 2000, pp. 703-706.			
	30.	Ruiz et al., "Design and Prototyping of DSP Custom Circuits Based on a Library of Arithmetic Components", Vol. 1, 9 November 1997, pp. 191-196.			
	31.	Tamiya, Y., "Delay Estimation for Technology Independent Synthesis", 1997 Proceedings of the ASP-DAC '97, Asia and South Pacific Design Automation Conference, 28 January 1997, pp. 31-36.			
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				Filing Date	1/31/02
				First Named Inventor	Steven Teig, et al.
				Group Art Unit	2825
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				Attorney Docket Number	SPLX.P0091

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	1.	5,311,442	05-10-1994	Fukushima	
	2.	5,526,276	06-11-1996	Cox et al	
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	12.	6,546,539	04-08-2003	Lu et al	

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	1.	5,519,630		05-21-1996	Nishiyama et al.	
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	7.	6,301,696	B1	11-09-2001	Lien et al.	

NON PATENT LITERATURE DOCUMENTS

Examiner* Initials	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ⁶
	8.	Crastes, M. et al., A Technology Mapping Method Based on Perfect and Semi-Perfect Matchings, Design Automation Conference, 1991, 28 th ACM/IEEE, June 17-21, 1991, pp. 93-98.	
	9.	Devadas, S. et al., Synthesis and Optimization for robustly delay-fault testable combinational logic circuits, Design Automation Conference, 1990, 27 th ACM/IEEE, June 24-28, 1990, pp. 221-227.	

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